REMARKS

Reconsideration and withdrawal of all outstanding issues, in consideration of this submission, is respectfully requested.

The amended title, it is submitted, is more aptly descriptive of the claimed invention. Therefore, reconsideration and withdrawal of the outstanding objection thereto is respectfully requested.

By the above-made amendments, claims 9-28 are now pending of which claims 9, 10 and 13-17 were amended and claims 18-28 are newly presented. Amendments were made to independent claims 9 and 13 for effecting further clarification of the subject matter to be covered including to highlight the particularities of applicants invention over that previously known including over the art documents as cited in the outstanding rejections. The nominal revision implemented in dependent claim 10 conforms to the revisions implemented in the base claim 9 thereof. The change implemented in each of dependent claims 14-16 is of an obvious, minor editorial nature. As to dependent claim 17, the change therein is also directed to an editorial clarification.

Claims 18-20 were added in consideration of more fully covering the various originally disclosed aspects directed to applicants invention. For example, dependent 18 is similar to that of claim 17 but is combined differently therefrom. Claim 19 further limits each interface circuit associated with a plug-in unit as being a part of the plug-in unit construction itself (see page 6, lines 8-11, of the Specification). Newly added dependent claim 20 further defines the "watchdog timer" of claim 10 as being provided at each interface circuit or at each plug-in unit (see Page 2, lines 27-31 and Page 6, line 19 et seq., of the Specification). Newly added claims 21-28 are based on that covered by claims 13-17 and 19 but, however, are formatted in the preamble somewhat differently.

The invention is a method for improving the reliability of a computer system which includes a bus and at least one plug-in unit coupled to the bus, the method comprising providing to each of at least one plug-in unit a separate interface circuit such that each plug-in unit is connected to the bus via a corresponding interface circuit; addressing a respective plug-in unit, via the bus, by addressing operations directed at the respective plug-in unit and which are monitored by the interface circuit corresponding thereto; performing a timed duration operation of addressing of the plug-in unit; and checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing, and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to that plug-in unit is terminated by the interface circuit corresponding thereto by sending into the bus a signal indicating termination of addressing. Claims 9-12 and 20 particularly set forth the method according to the present invention. Supportive discussion directed thereto can be found in connection with the example flowchart shown in Fig. 3 of the drawings and the related discussion on page 9, line 34 et seq. of the Specification. Additional discussion is found on page 3, line 7 et seq. and line 26 et seq. and the description regarding Figs. 1a, 1b and 2, as examples thereof only. Regarding dependent claims 11 and 12, for example, see the example related discussion on Page 7, line 22 et seq. and line 29 et seq. of the Specification.

According to a further aspect thereof, the invention sets forth an interface circuit for providing local-monitoring (e.g., self-monitoring) capability to a plug-in unit of a computer system including a bus and at least one plug-in unit coupled to the bus, wherein a separate interface circuit is provided for and to connect each said

plug-in unit to the bus and comprising a watchdog timer; first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto; and second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of the addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer. Claims 13-19 set forth such an interface circuit scheme with regard to improving the reliability of the computer system. The invention according to newly presented claims 21-28 likewise sets forth an interface circuit scheme with regard to an improved computer system. Regarding the set forth "watchdog timer", examples thereof are shown with regard to Figs. 1 and 2 of the drawings and as also discussed on page 6, line 19 etc. Regarding the set forth "first means", the discussion on page 6, lines 33 et seq is just one example illustration thereof such as it relates to Fig. 1B. Regarding the set forth "second means", an example discussion thereof is found on page 3, line 14 et seq. as well as on page 7, line 11 et seq. of the present Specification, although not limited thereto.

The present invention, for example, has been further clarified to highlight that the respective plug-in units which are connected, for example, to a PCI bus such as a Compact PCI bus in a computer are monitored locally, i.e., the plug-in units, in effect, operate as if they contain a self-monitoring feature. In this regard, a respective plug-in unit which is connected to, for example, a compact PCI bus or a respective interface circuit acting as the interface between the bus and the plug-in unit is provided with a watchdog timer for internal monitoring of the addressing of that plug-in unit. This therefor makes it possible to detect error situations that are more quickly detectable and allow for the automatic releasing of, for example, a defective plug-in unit such as a peripheral unit of a computer system.

According to the outstanding Office Action, claims 9-17 stand rejected under 35 USC §102(e) as anticipated by Porterfield (USP 6,349,347). As will be shown, hereinbelow, in conjunction with the above discussion, the invention according to claims 9-17, as now amended, and that according to newly presented claims 18-28 was neither disclosed nor suggested by Porterfield. Therefore, insofar as presently applicable, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

Porterfield discloses a method for configuring peer devices without additional delay such as during boot-up, for example, in a personal computer system (see Col. 3, line 20 et seq.). Although one can consider Porterfield's technique as an improvement in the reliability of a computer system, as alleged in the rejection, Porterfield's technique appears to be directed moreso to improving the usability and user-friendliness of the PC. This is evident from the fact that Porterfield talks about the desire to expedite the configuration cycles without causing the system failure and that his technique is particularly concerned during the initiating or boot-up phase of the PC and the easiness with regard to use of the compatibility bridge 220 to facilitate an easier, i.e., a more user friendly peer device configuring. As can be seen from Fig. 2 in Porterfield, a CPU 200 is connected to a host bus 210 to communicate control and data signals to and from other devices on the host bus. Typically, there are also one or more PCI-PCI bridges, which may be considered as a peer device, connected to the host bus. When one or more such PCI-PCI bridge is present, one of them can be selected as the "compatibility" bridge (e.g., compatibility bridge 220).

From Fig. 2 in Porterfield, the compatibility bridge 220 connects two different host busses. Moreover, it also takes care of signaling the configuration cycles between these two busses. If it is aware of a malfunction of one or more of the peer

devices connected to the bus, it terminates the signaling of the faulty peer device and thus prevents the malfunction in the system startup for example. In this regard, when a configuration cycle is initiated to a particular device, the compatibility bridge 220 checks the logical state of the bit corresponding to that device in the scorecard register 224. If the bit is set to logic 1, the compatibility bridge 220 forwards the configuration cycle to the PCI bus 230. If the bit is clear (that is, set to logic 0), the compatibility bridge 220 does not claim the cycle on the host bus 210 and, hence, does not forward the configuration cycle to the PCI bus 230. Accordingly, the compatibility bridge 220 allows another peer device to claim the configuration cycle on the host bus 210 (see Col. 4, lines 35-45). Consistent with Porterfield's technique, also, if the compatibility bridge 220 does not receive any response from the peer device, it becomes aware of its malfunction and makes a note directed thereto into a predetermined look up table (e.g., status register 226) of the compatibility bridge 220.

Based on Porterfield's technique including, for example, the Fig. 2 embodiment thereof, the above referred to steps regarding the configuring of peer devices are performed by one and the same device, namely, the compatibility bridge 220. In other words, Porterfield disclosed a technique requiring a centralized solution for improving the system initialization procedure. According to Porterfield, the compatibility bridge 220 monitors a plurality of other peer devices, in clear contradistinction with that set forth in claims 9+, 13+ and 21+.

According to the invention set forth in independent claims 9, 13 and 21, each of the plug-in units is monitored locally, i.e., each has a self-monitoring capability through the action of, for example, the watchdog timer and interface circuit (the interface circuit may contain the watchdog timer). As can be seen from each of the independent claims, a separate interface circuit is connected to each of the plug-in

units. With regard to claim 1, for example, the method also calls for the addressing operations which are targeted for a respective plug-in unit are monitored by the interface circuit corresponding to that plug-in unit. Such, it is submitted, was not disclosed nor, for that matter, even suggested by Porterfield. The interface circuit corresponding to a plug-in unit, according to the present invention, may be a part of the plug-in unit itself (see claims 19 and 27 and page 6, lines 8-11, of the Specification). It is emphasized, addressing operations directed at any individual plug-in unit are monitored by the corresponding interface circuit connected thereto, which is in clear contradistinction with Porterfield's centralized monitoring scheme. Consistent with that presently set forth, if the interface circuit detects that the duration operation of addressing exceeds the predetermined time period, i.e., it exceeds the time limit of the preset addressing cycle, it terminates the addressing by sending into the bus a signal indicating the termination of addressing (e.g., SERR# signal, see page 7, line 22 et seq., of the Specification).

In order to understand the improvements realized with regard to the present invention, the following brief discussion addresses problems which the present inventors addressed which led to the achieving of the present invention. Plug-in units connected to the bus communicate with each other by using a special addressing sequence. In certain addressing sequences, an addressing unit addresses a unit to be addressed or waits for a response to the addressing until the addressed unit responds. If the unit addressed is defective, it is unable to respond to the addressing, in which case the entire computer or microcomputer system will remain waiting for the release of the address bus. This may lead to an error situation in the entire system. An example of this type of situation arises in certain addressing modes of the Compact PCI bus in which the addressing sequence does not include any element for the monitoring of bus release. Under these conditions,

a problem arises if the plug-in unit is defective, in which case it may, acting via an interface circuit, keep the device select signal or DEVSEL # signal of the Compact PCI bus active and the target ready signal or TRDY # signal inactive, thus indicating that it is aware of being addressed (DEVSEL #) but is not yet ready for action. The system controlling the PCI bus remains waiting for the release of the BUS and the operation of the system is thus locked up. (See the discussion in the Background section of the present Specification, for example, on page 1, line 21 to page 2, line 6). As also discussed in background information in the present Specification (see Page 2, lines 7-15), typically, the master unit of the system is provided with a so-called watchdog timer, which has to be reset at certain predetermined intervals. If the watchdog timer is not reset, then the system will be prompted to reboot, i.e., reset itself. This may lead to an endless loop as well as a crash of the system. However, in the above discussed example, the watchdog timer is not necessarily started at all, or it may "notice" the problematic situation that has arisen.

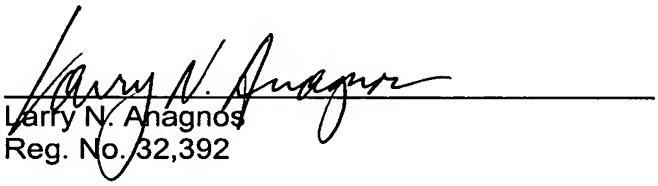
It is submitted, for at least the above reasons, the invention according to claims 9+,13+ and 21+ could not have been anticipated nor, for that matter, rendered obvious from Porterfield's teachings. There is neither explicit teaching nor suggestion by Porterfield that would have led one of ordinary skill in the art to achieve the present invention in the manner as that presently set forth in the claims. A key reason (although not limited thereto) is that Porterfield's disclosure specifically teaches a solution which requires a centralized system for monitoring the peer devices. Also, the improved scheme achieved by the present inventors is a clear improvement over that previously known and especially over the teachings of Porterfield. For example, each of the plug-in units is, in effect, able to self-monitor itself. Therefore, it would be significantly cheaper as well as more practical to accomplish a plug-in unit configuration scheme for a computer system in a manner

as presently set forth as there would be no need to make major changes to the computer system itself but, rather, it would simply require the replacement or bypassing of a plug-in unit.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding objection to the title and rejection to the claims as well as favorable action on all of the presently pending claims, i.e., claims 9-28, and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (1154.41135X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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